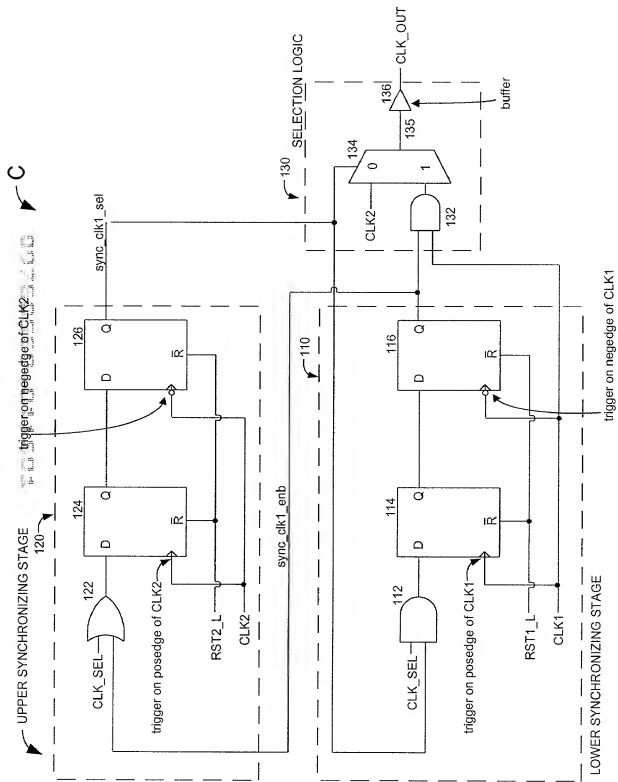


FIG. 1



**Notes:**

- \* RST2\_L is system reset synchronized to CLK2.
- \* RST1\_L is system reset synchronized to CLK1.
- \* CLK\_SEL is an asynchronous signal.

**Figure 2a**

Synthesized (gate implementation) schematic from Verilog RTL

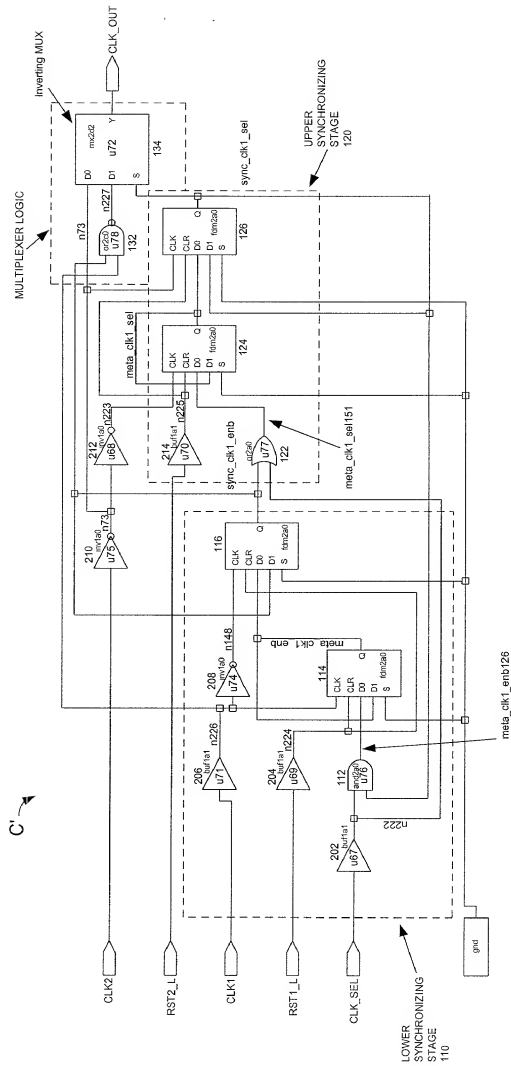
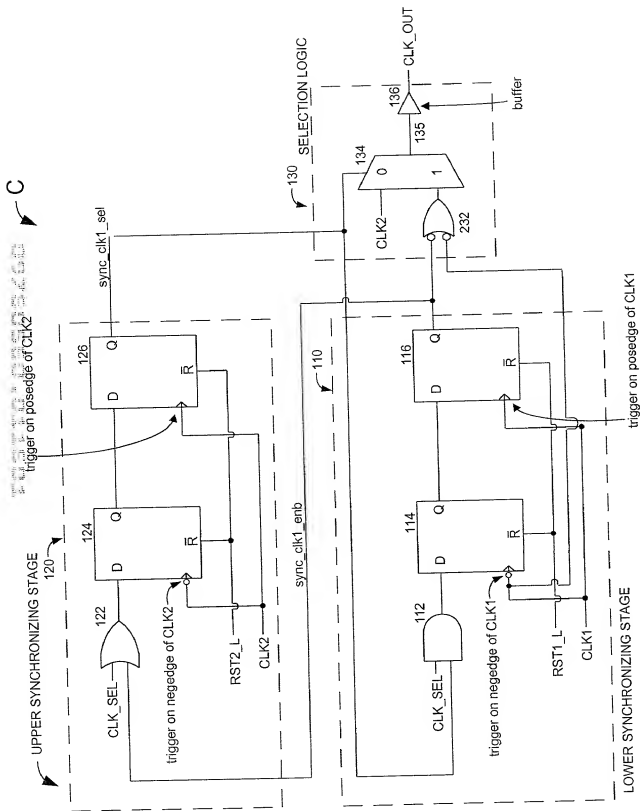


Figure 2b



**Notes:**

- \* RST2\_L is system reset synchronized to CLK2.
- \* RST1\_L is system reset synchronized to CLK1.
- \* CLK\_SEL is an asynchronous signal.

**Figure 2c**

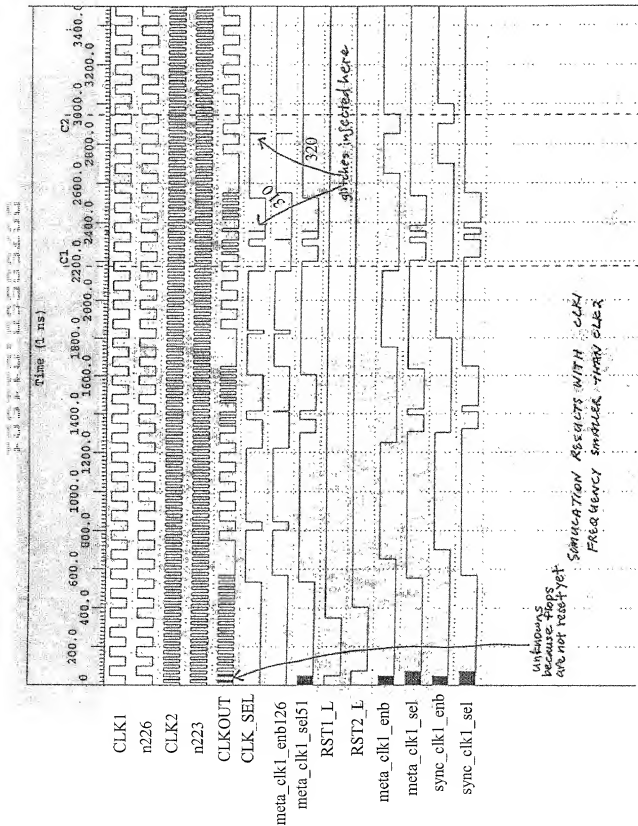


Figure 3

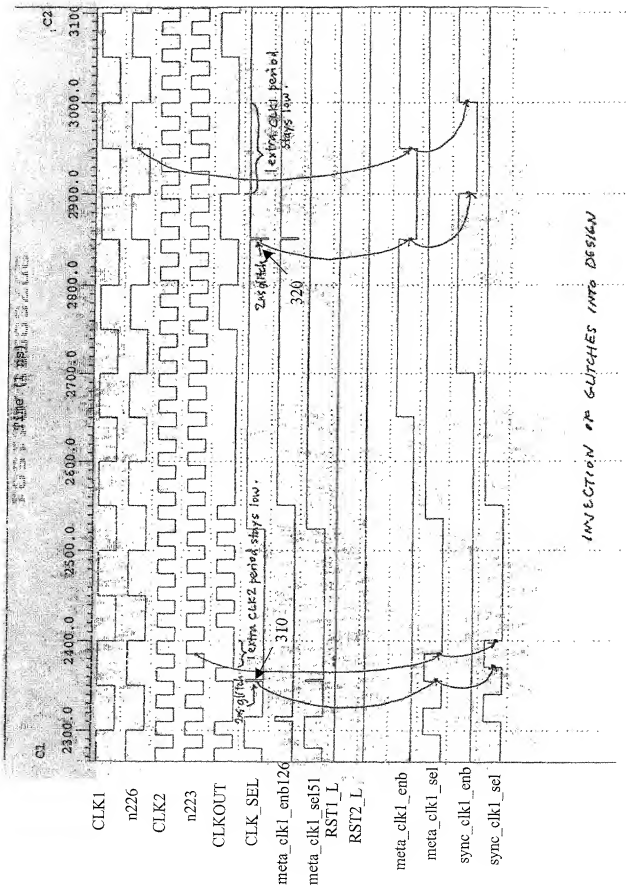


Figure 4

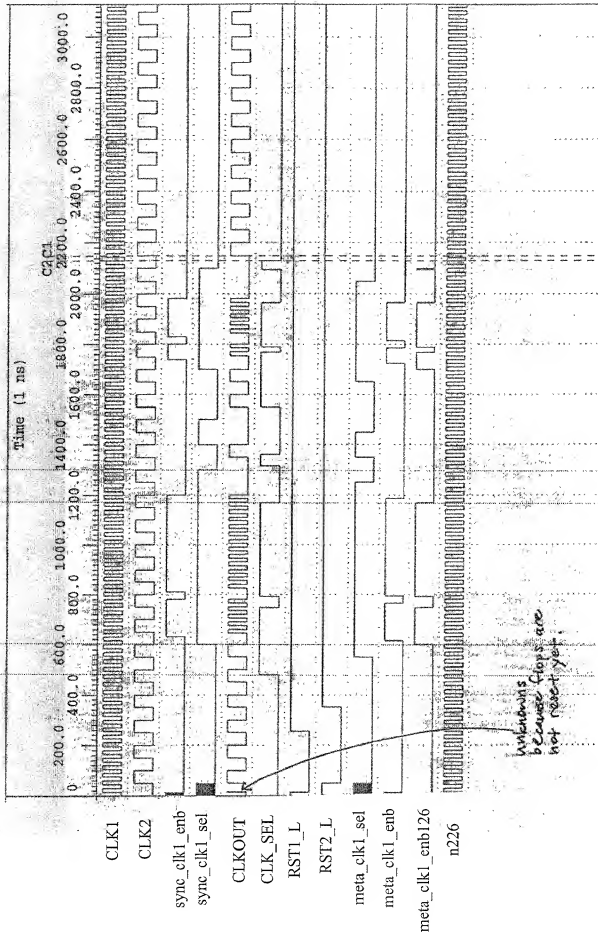


Figure 5

T1 T2 T3 T4